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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,074	09/18/2003	Chun-Liang Lee	LA-7196-129.US	6848
167	7590	03/06/2006	EXAMINER	
FULBRIGHT AND JAWORSKI LLP 555 S. FLOWER STREET, 41ST FLOOR LOS ANGELES, CA 90071			STIGLIC, RYAN M	
			ART UNIT	PAPER NUMBER
			2112	

DATE MAILED: 03/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/667,074	Applicant(s) LEE, CHUN-LIANG	
	Examiner Ryan M. Stiglic	Art Unit 2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 December 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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DETAILED ACTION

1. Claims 1-13 are pending and have been examined.
2. Claims 1-13 are rejected.

Response to Arguments

3. Applicant's arguments filed 30 December 2005 have been fully considered but they are not persuasive. The Claim for Priority has not been entered because it fails to adhere to the guidelines set forth in MPEP § 201.14, **Right of Priority, Formal Requirements**. MPEP § 201.14 reads as follows:

For original applications filed under 35 U.S.C.111(a) (other than a design application) on or after November 29, 2000, the requirements of the statute are that the applicant must (a) file a claim for the right of priority and (b) identify the original foreign application by specifying the application number of the foreign application, the intellectual property authority or country in which the application was filed and the date of filing of the application. These papers must be filed within a certain time limit. The time limit specified in 35 U.S.C. 119(b)(1) is that the claim for priority and the required identification information must be filed at such time during the pendency of the application as set by the *>Director<. The *>Director< has by rule set this time limit as the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. See 37 CFR 1.55(a)(1)(i). This time period is not extendable. In an application that entered the national stage from an international application after compliance with 35 U.S.C. 371, the claim for priority must be made during the pendency of the application and within the time limit set forth in the PCT and the Regulations under the PCT. See 37 CFR 1.55(a)(1)(ii). Claims for foreign priority not presented within the time period specified in 37 CFR 1.55(a)(1)(i) are considered to have been waived. If a claim for priority under 35 U.S.C. 119(a) - (d) or (f), or 365(a) is presented after the time period set in 37 CFR 1.55(a)(1)(i), the claim may be accepted if it includes the required identification information and is accompanied by a grantable petition to accept the unintentionally delayed claim for priority. See 37 CFR 1.55(c). In addition, 35 U.S.C. 119(b)(3) gives the *>Director< authority to require a certified copy of the foreign application and an English translation if the foreign application is not in the English language and such other information as the *>Director< may deem necessary. The *>Director< has by rule, 37 CFR 1.55(a)(2), required a certified copy of the foreign application to be submitted before the patent is granted. If the certified copy of the foreign application is submitted after the payment of the issue fee, it must be accompanied by the processing fee set forth in 37 CFR 1.17(i). See MPEP § 201.14(a). Unless provided in an application data sheet, 37 CFR 1.63 requires that the oath or declaration must identify the foreign application for patent or inventor's certificate for which priority is claimed under 37 CFR 1.55, and any foreign applications having a filing date before that of the application on which priority is claimed, by specifying the application number, country, day, month, and year of its filing.

37 CFR 1.55 *Claim for foreign priority* reads as follows:

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(a) An applicant in a nonprovisional application may claim the benefit of the filing date of one or more prior foreign applications under the conditions specified in 35 U.S.C. 119(a) through (d) and (f), 172, and 365(a) and (b).

(1)(i) In an original application filed under 35 U.S.C. 111(a), the claim for priority must be presented during the pendency of the application, and within the later of four months from the actual filing date of the application or sixteen months from the filing date of the prior foreign application. This time period is not extendable. The claim must identify the foreign application for which priority is claimed, as well as any foreign application for the same subject matter and having a filing date before that of the application for which priority is claimed, by specifying the application number, country (or intellectual property authority), day, month, and year of its filing. The time periods in this paragraph do not apply in an application under 35 U.S.C. 111(a) if the application is:

(A) A design application; or

(B) An application filed before November 29, 2000.

(ii) In an application that entered the national stage from an international application after compliance with 35 U.S.C. 371, the claim for priority must be made during the pendency of the application and within the time limit set forth in the PCT and the Regulations under the PCT.

(2) The claim for priority and the certified copy of the foreign application specified in 35 U.S.C. 119(b) or PCT Rule 17 must, in any event, be filed before the patent is granted. If the claim for priority or the certified copy of the foreign application is filed after the date the issue fee is paid, it must be accompanied by the processing fee set forth in § 1.17(i), but the patent will not include the priority claim unless corrected by a certificate of correction under 35 U.S.C. 255 and § 1.323

**>

(3) The Office may require that the claim for priority and the certified copy of the foreign application be filed earlier than provided in paragraphs (a)(1) or (a)(2) of this section:

(i) When the application becomes involved in an interference (see § 41.202 of this title),

(ii) When necessary to overcome the date of a reference relied upon by the examiner, or

(iii) When deemed necessary by the examiner.

(4)(i) An English language translation of a non-English language foreign application is not required except:

(A) When the application is involved in an interference (see § 41.202 of this title),

(B) When necessary to overcome the date of a reference relied upon by the examiner, or

(C) When specifically required by the examiner.

(ii) If an English language translation is required, it must be filed together with a statement that the translation of the certified copy is accurate.<

(c) Unless such claim is accepted in accordance with the provisions of this paragraph, any claim for priority under 35 U.S.C. 119(a)-(d) or 365(a) not presented within the time period provided by paragraph (a) of this section is considered to have been waived. If a claim for priority under 35 U.S.C. 119(a)-(d) or 365(a) is presented after the time period provided by paragraph (a) of this section, the claim may be accepted if the claim identifying the prior foreign application by specifying its application number, country (or intellectual property authority), and the day, month, and year of its filing was unintentionally delayed. A petition to accept a delayed claim for priority under 35 U.S.C. 119(a)-(d) or 365(a) must be accompanied by:

(1) The claim under 35 U.S.C. 119(a)-(d) or 365(a) and this section to the prior foreign application, unless previously submitted;

(2) The surcharge set forth in § 1.17(t); and

(3) A statement that the entire delay between the date the claim was due under paragraph (a)(1) of this section and the date the claim was filed was unintentional. The Director may require additional information where there is a question whether the delay was unintentional.

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In accordance with MPEP § 214.04, applicant must submit: (a) a petition under 37 CFR 1.55(c); (b) a new oath/declaration or application data sheet; (c) fee set forth in 37 CFR 1.17; and (d) a statement that the entire delay between the date the claim was due and the date the claim was filed was unintentional

4. Insofar as applicant's claim for foreign priority under 35 U.S.C. §119 does not adhere to the guidelines set forth in MPEP §201.14 and 37 CFR §1.55 such priority can not be granted at this time. As such the prior art rejections dated August 31, 2005 are maintained and provided below.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-4, 6, 8-10, and 12-13 are rejected under 35 U.S.C. 102(a) as being anticipated by the Intel Server Chassis SBCE and its various components available at least on August 2003 as evidenced by the article titled "Can a blade solve my computer server needs".

a. The evidentiary art proves that the Intel Server Chassis SBCE and its various components were publicly available at least by August 2003. The various components of the SBCE chassis include the Intel Server Compute blade SBXL52 and the Intel Server Management module SBCECM. The SBXL52 Server Blade is functionally equivalent

to the server of applicant's invention and references to features of applicant's servers will be made with respect to the SBXL52. Also, the SBCECMM is functionally equivalent to the switching device of applicant's invention and references to features of applicant's switching device will be made with respect to SBCECMM.

b. Independent claims 1 and 8 are substantially equivalent in that claim 8 is drawn to the method of operating the system of claim 1, therefore claim 8 is rejected on the same basis as those reasons disclosed below with respect to claim 1. Like wise all claims dependent upon claim 8 are substantially equivalent to claim 1 and its dependent claims as associated below.

c. Regarding claims 1 and 8, the Intel Server Chassis SBCE discloses:

- An input/output (I/O) unit access switching system (SBCE Server Chassis), comprising:
- a plurality of servers (observe cover of article titled "Can a blade solve my computer server needs?) each comprising a control module (article titled "Intel® Server Compute Blade SBXL52"; page 2, "Front Panel Buttons") and an intelligent platform management interface (IPMI) having a baseboard management controller (BMC) (article titled "Intel® Server Compute Blade SBXL52"; page 1, "Features: ...Onboard baseboard management controller [BMC]...Benefits: ...Monitor and control server blade remotely, increasing server uptime and lowering management costs...");

- at least one input device (White paper titled “Simplifying Complexity Blades Management in the Data Center”; page 7, “Remote and local KVM...”);
- at least one output device (White paper titled “Simplifying Complexity Blades Management in the Data Center”; page 7, “Remote and local KVM...”); and
- a switching device (Intel SBCECMM) comprising a microprocessor unit (Manual titled “Intel® Server Management Module SBCECMM: Installation and User’s Guide”; page 1, “The service processor in the management module...”), an input function switching unit connected to the microprocessor unit (White paper titled “Simplifying Complexity Blades Management in the Data Center”; page 7, “...using the built-in KVM switch...”; Manual titled “Intel® Server Management Module SBCECMM: Installation and User’s Guide”; page 1, “...and a keyboard/video/mouse (KVM) multiplexor...” and each of the BMCs (please see below) , an output function switching unit connected to the microprocessor unit and each of the servers unit (White paper titled “Simplifying Complexity Blades Management in the Data Center”; page 7, “...using the built-in KVM switch...”; Manual titled “Intel® Server Management Module SBCECMM: Installation and User’s Guide”; page 1, “...and a keyboard/video/mouse (KVM) multiplexor...”), an interrupt unit connected to the microprocessor unit and each of the BMCs (the interrupt unit is inherently present in the Intel SBCECMM as will be described below), at least one set of input connection ports connected to the microprocessor unit and the input device (White paper titled “Simplifying Complexity Blades Management in the Data Center”; Cover Sheet shows the Intel SBCECMM with 3

input ports, a keyboard, a mouse, and a LAN port ; page 7, "...using the built-in KVM switch..."; Manual titled "Intel® Server Management Module SBCECMM: Installation and User's Guide"; page 1, "...and a keyboard/video/mouse (KVM) multiplexor..."), and at least one set of output connection ports connected to the microprocessor unit and the output device (White paper titled "Simplifying Complexity Blades Management in the Data Center"; Cover Sheet shows the Intel SBCECMM with an RGB video output ; page 7, "...using the built-in KVM switch..."; Manual titled "Intel® Server Management Module SBCECMM: Installation and User's Guide"; page 1, "...and a keyboard/video/mouse (KVM) multiplexor...");

- wherein when the control module of one of the servers is activated, the BMC of the corresponding server outputs an interrupt request signal to the interrupt unit of the switching device, so as to allow the interrupt unit to determine if the interrupt request signal is transmitted from the server whose control module is activated, and to forward the determination result to the microprocessor unit, whereby the microprocessor unit generates an input switch request signal that is transmitted to the input function switching unit, and generates an output switch request signal that is transmitted to the output function switching unit, such that according to the input and output switch request signals respectively, the input function switching unit and the output function switching unit each generates and transmits a corresponding switch driving signal to the BMC of the server whose control module is activated, and such that this server who receives the switch driving

signals is allowed to receive an input signal from the input device through the corresponding BMC, the input function switching unit and the input connection ports, and to consequently execute operations according to the input signal, as well as to output the operational result to the output device through the output function switching unit and the output connection ports (article titled “Intel® Server Compute Blade SBXL52”; page 2, “Front Panel Buttons... This button is for associating the keyboard port, mouse port, and video port with this blade server; the LED on this button flashes while the request is being processed, then is steady when ownership has been transferred to the blade server...”).

- d. When a user of the Intel SBCE Server Chassis requires keyboard/video/mouse access to a particular server blade of the chassis, they simply press a button on the front of the blade server (article titled “Intel® Server Compute Blade SBXL52”; page 2, “Front Panel Buttons... This button is for associating the keyboard port, mouse port, and video port with this blade server; the LED on this button flashes while the request is being processed, then is steady when ownership has been transferred to the blade server...”). The recited paragraph discloses an LED associated with the blade server flashes while the request for keyboard/video/mouse ownership is being processed. The Examiner understands this request to be equivalent to the sending of an interrupt upon pressing the control module since the SBCECMM of the server chassis is the only device mentioned in the system to have an “Integrated KVM switch” (article titled “Intel Server Management for Blades” page 2). In other words, since the SBCECMM is the only

module in the SBCE server chassis with an integrated KVM switch, all interrupts/requests for input/output port access must be handled by SBCECMM. Furthermore the manual titled “Intel® Server Management Module SBCECMM: Installation and User’s Guide” discloses (page 1), “The service processor in the management module communicates with the service processor (BCM) in each blade server for such functions as: ...Blade server requests for keyboard, mouse, and video.” Therefore the blade servers must communicate an interrupt/request to the SBCECMM/switching device (more specifically the microprocessor of) to be given input/output port ownership. Internal signals of the SBCECMM instructing the built-in KVM switch to switch the input/output ports to a given blade server must also be present in order for the SBCECMM to function as described in various references. Also, a previously recited passage stated that the LED associated with a blade server’s input/output port request will flash while the request is being processed and then remain lit steadily “when ownership has been transferred to the blade server.” Therefore, it is an inherent feature of the SBCE Server chassis that upon completion of the input/output port switching the service processor of the SBCECMM must inform the blade server that it has ownership of the ports. This is supported by the LED staying constantly lit when ownership of the input/output ports has been transferred to the blade server.

- e. Regarding 2, the Intel Server Chassis SBCE discloses: The I/O unit access switching system of claim 1, wherein the input connection port is connected to a

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keyboard or mouse (White paper titled “Simplifying Complexity Blades Management in the Data Center”; Cover Sheet shows the Intel SBCECMM with 3 input ports, a keyboard, a mouse, and a LAN port ; page 7, “...using the built-in KVM switch...”; Manual titled “Intel® Server Management Module SBCECMM: Installation and User’s Guide”; page 1, “...and a keyboard/video/mouse (KVM) multiplexor...”).

f. Regarding claim 3, the Intel Server Chassis SBCE discloses: The I/O unit access switching system of claim 1, wherein the output connection port is connected to a monitor (White paper titled “Simplifying Complexity Blades Management in the Data Center”; Cover Sheet shows the Intel SBCECMM with 1 RGB video output port that is to be connected to a monitor ; page 7, “...using the built-in KVM switch...”; Manual titled “Intel® Server Management Module SBCECMM: Installation and User’s Guide”; page 1, “...and a keyboard/video/mouse (KVM) multiplexor...”).

g. Regarding claim 4, the Intel Server Chassis SBCE discloses: The I/O unit access switching system of claim 1, wherein the control module is a switch (article titled “Intel® Server Compute Blade SBXL52”; page 2, “Front Panel Buttons”; A button is a type of switch).

h. Regarding claim 6, the Intel Server Chassis SBCE discloses: The I/O unit access switching system of claim 1, wherein the output function switching unit is a multiplexer (White paper titled “Simplifying Complexity Blades Management in the Data Center”;

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Cover Sheet shows the Intel SBCECMM with 1 RGB video output port that is to be connected to a monitor ; page 7, "...using the built-in KVM switch..."; Manual titled "Intel® Server Management Module SBCECMM: Installation and User's Guide"; page 1, "...and a keyboard/video/mouse (KVM) multiplexor...").

i. Regarding claim 9, the Intel Server Chassis SBCE discloses: The I/O unit access switching method of claim 8, wherein each of the servers has a control module for generating the request for access to the I/O devices (please see section 4 subsection d above).

j. Regarding claim 10, the Intel Server Chassis SBCE discloses: The I/O unit access switching method of claim 9, wherein the control module is a switch (please see section 4 subsection g).

k. Regarding claim 12, the Intel Server Chassis SBCE discloses: The I/O unit access switching method of claim 8, wherein the I/O devices include an input device that is a keyboard or mouse (please see section 4 subsection e).

l. Regarding claim 13, the Intel Server Chassis SBCE discloses: The I/O unit access switching method of claim 8, wherein the I/O devices include an output device that is a monitor (please see section 4 subsection f).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 5, 7, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the Intel Server Chassis SBCE as applied to claims 1 and 8 above, and further in view of the I²C Specification (January 2000).

As discussed above, the Intel Server Chassis SBCE teaches of a server blade (SBXL52) with a front panel button used to send an interrupt/request to a service processor within a switching device (SBCECMM) such that the service processor instructs an embedded KVM switch to associate the input/output ports of the Chassis to the particular blade server whose button/switch was pressed. The Intel Server Chassis further teaches USB is used to communicate input/output signals (from the keyboard, video [of the server blade], or mouse) from the server blade (SBXL52) and the switching device (SBCECMM) (manual titled "Intel® Server Chassis SBCE: Installation and User's Guide"; page 21). The Intel Server Chassis fails to teach internal communications between the input/output devices and the server blades adhering to the I²C protocol.

The I²C Specification teaches the I²C is an excellent choice for device communication because:

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- Only two bus lines are required; a serial data line (SDA) and a serial clock line (SCL)
- Each device connected to the bus is software addressable by a unique address and simple master/slave relationships exist at all times; masters can operate as master-transmitters or as master-receivers
- Design-time reduces as designers quickly become familiar with the frequently used functional blocks represented by I2C-bus compatible ICs
- ICs can be added to or removed from a system without affecting any other circuits on the bus
- Fault diagnosis and debugging are simple; malfunctions can be immediately traced (page 4)

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the communication bus between the SBCECMM integrated KVM switch and the SBXL52 blade server service processor as an I²C bus because the simple 2-wire serial I2C-bus minimizes interconnections so ICs have fewer pins and there are not so many PCB tracks; result - smaller and less expensive PCBs.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

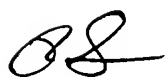
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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday - Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571.272.3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).




PAUL R. MYERS
PRIMARY EXAMINER